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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,548	04/02/2004	Martin Ceredig Roberts	MI22-2550	2546
21567	7590	10/04/2005	EXAMINER	
WELLS ST. JOHN P.S. 601 W. FIRST AVENUE, SUITE 1300 SPOKANE, WA 99201			PERALTA, GINETTE	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/817,548	ROBERTS ET AL.	
	Examiner	Art Unit	
	Ginette Peralta	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 July 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 55-67 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 55-67 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

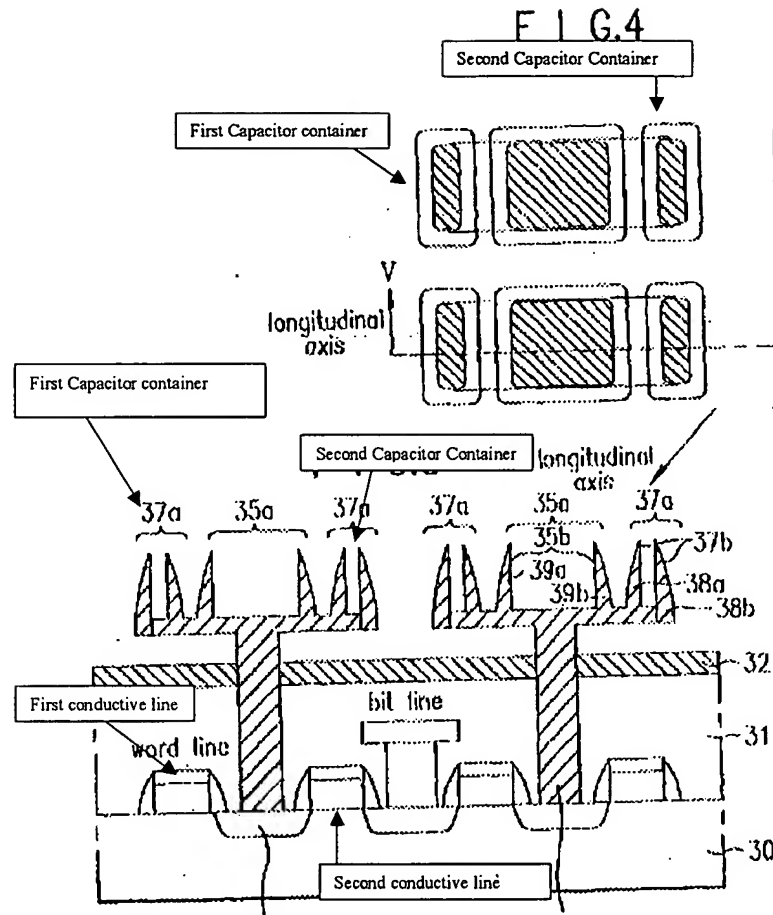
1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 55-58 and 62-67 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Cho (U. S. Pat. 6,448,145 B2).

Regarding claim 55, Cho discloses in Figs. 3a-3e a method of forming a capacitor that comprises providing a substrate 30 having a node location 30a disposed between a first conductive line (*word line*) and a second conductive line (*word line*); forming a contact structure 34 in electrical communication with the node location 30a, the contact structure 34 extending laterally over at least a portion of each of the conductive lines (*word line*) as shown in Fig. 3c; and forming capacitor containers 37a in electrical communication with the node location 30a, the capacitor containers 37a consisting of a first container 37a disposed at least partially over a only the first conductive line (*word line*) and a second container 37a disposed at least partially over only the second conductive line (*word line*), the first container 37a being spaced from the second capacitor container 37a as shown in Figs. 4 and 5.

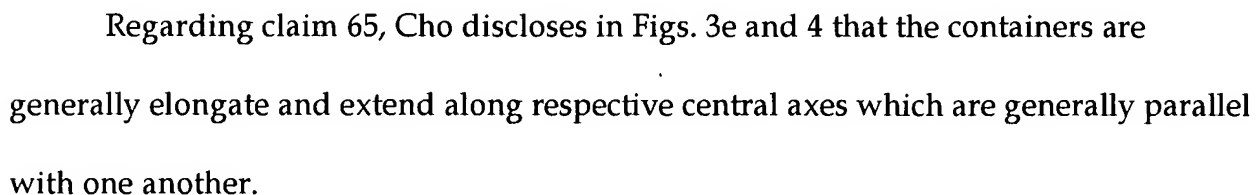


Regarding claim 56, Cho discloses in Figs. 3a-3e that the method of forming the capacitors comprises forming a masking layer 36 over the substrate 30 and over the conductive lines (*word line*); forming a first opening within the masking layer 36 over the first conductive line; forming a second opening within the masking layer 36 over the second conductive line; and depositing a conductive material 37 within the first and second openings, the conductive material being in direct physical contact with the contact structure 34.

Regarding claim 57, Cho discloses in col. 6, lines 24-31, that the conductive material 37 comprises polysilicon.

Regarding claim 58, Cho discloses in col. 6, lines 32-39 that the method further comprises lining the capacitor containers with a dielectric material 39; and forming a capacitor electrode layer 40 over the dielectric material and within the first and second containers 37a.

Regarding claim 62, Cho discloses in Figs. 3a-3e a method of forming a DRAM circuitry that comprises providing a substrate 30 having a first and second spaced apart node locations 30a; forming a first storage capacitor in electrical communication with the first node location 30a and comprising capacitor containers consisting of first and second containers 37a, the first container being at least partially disposed over a first conductive line (*word line*), the second container being disposed at least partially over a second conductive line (*word line*); forming a second storage capacitor in electrical communication with the second node location 30a and comprising capacitor containers consisting of third and fourth containers 37a, the third container being at least partially disposed over a third conductive line (*word line*), the fourth container being disposed at least partially over a fourth conductive line (*word line*); lining the first, second, third, and fourth containers with a dielectric layer 39; and depositing a conductive capacitor electrode layer 40 over the dielectric layer 39 and within the containers.



Regarding claim 66, Cho discloses in Figs. 3e and 4 that the containers are generally elongate and extend along respective central axes, and wherein each container comprises a respective portion which has a generally circular transverse cross section.

Regarding claim 67, Cho discloses in Figs. 3e and 4 that each container 37a has a volume which is substantially equivalent relative to each other.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 59-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho in view of Hermes (U. S. Pat. 6,596,577 B2).

Regarding claim 59, Cho discloses in Figs. 3a-3e a method of forming a capacitor that comprises providing a substrate 30 having a node location 30a; forming a contact structure 34 in electrical communication with the substrate node location 30a, the contact structure 34 being disposed between two conductive lines (*word line*), extending elevationally above and laterally outward over the two conductive lines (*word line*) as shown in Fig. 3c; forming a first capacitor container 37a having a continuous conductive layer 37 defining a first interior area, the conductive layer being joined with the contact

structure 34, the first container 37a being disposed at least partially over one of the conductive lines (*word line*); forming a second container 37a having a continuous conductive layer 37 defining a second interior area, the conductive layer being joined with the contact structure 34, the first and second interior areas being spaced apart from one another in a non-overlapping relationship, as shown in Fig. 4; and forming a dielectric layer and a conductive capacitor electrode layer disposed operably proximate the first container, the second container, and portions of the contact structure 34, as disclosed in col. 6, lines 32-39.

Cho discloses the claimed invention with the exception of the contact structure contacting an uppermost surface of each of the two conductive lines.

Hermes discloses in Figs. 1-10 a method of forming a capacitor structure that comprises providing a substrate 22 having a substrate node location 38; forming a contact structure 54 in electrical communication with the substrate node location 38, the contact structure being disposed between two conductive lines (*26 and 28*), extending elevationally above and laterally outward over and contacting an uppermost surface of each of the two conductive lines (*26 and 28*); forming a first container having a continuous conductive layer 62 defining a first interior area (*as shown in Fig. 6*), the conductive layer being joined with the contact structure 54, the first container being disposed at least partially over one of the two conductive lines 26; and forming a dielectric layer 64 and a conductive capacitor electrode layer 66 disposed operably proximate the first container, and portions of the contact structure 54, as disclosed in

Fig. 6, wherein the contact structure is formed extending elevationally above and laterally outward over and contacting an uppermost surface of each of the conductive lines for the disclosed intended purpose of including reductions in the processing steps required to form circuitry, as well as reductions in concerns associated with under- and over-etching substrate portions during fabrication as disclosed in col. 5, lines 24-30.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the contact structure of Cho extending elevationally above and laterally outward over and contacting an uppermost surface of each of the conductive lines for the disclosed intended purpose of Hermes of including reductions in the processing steps required to form circuitry, as well as reductions in concerns associated with under- and over-etching substrate portions during fabrication as disclosed in col. 5, lines 24-30. .

Regarding claim 60, Cho discloses in Fig. 3e that the containers are elongate and extend along generally parallel central axes.

Regarding claim 61, Cho discloses in Fig. 3e that the capacitor containers 37a are laterally separated by a dielectric region 39, and at least one of the containers being elongate and generally tubular in shape as shown in Fig. 4.

Response to Arguments

5. Applicant's arguments filed 7/20/05 have been fully considered but they are not persuasive.

Regarding applicant's argument that Cho does not disclose the claimed invention since Cho teaches in col. 6, ll. 41-46 and Figs. 4 and 5 that the structure includes storage node electrodes each having a cylindrical structure in which three cylinders overlap per storage node in a longitudinal axis direction and two cylinders overlap in the transverse axis direction, it is noted that as shown in Figs. 4 and 5, the outer cylinders do not overlap with each other, but rather they each overlap with a centermost cylinder in the longitudinal axis and in the transverse axis of Figs. 4 and 6 it is two capacitors that are shown along the storage node and the two separate capacitors outermost containers are the ones overlapping as disclosed in Figs. 4 and 6 and in col. 5, ll. 27-31.

6. Applicant's arguments with respect to claims 59-61 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the


shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571) 272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GP


HOAI PHAM
PRIMARY EXAMINER